AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 4, line 16 with the following paragraph:

Referring to FIG. 1, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented to (i) transfer data from one clock domain to another clock domain and (ii) indicate when data is ready for further processing (e.g., valid) from one clock domain to another clock domain. In one example, the circuit 100 may be implemented integral to a synchronous digital application specific integrated circuit (ASIC), complex programmable logic device (CPLD) or field programmable gate array (FPGA) 101. However, the circuit 100 may be implemented in any appropriate logic and/or circuitry accordingly to meet the design criteria of a particular application.

Please replace the paragraph beginning on page 24, line 2 with the following paragraph:

~~A~~ An apparatus including a first circuit and a second circuit. The first circuit may be configured to present a first data signal and a first indicator signal in response to a first clock signal and an enable signal. The second circuit may be configured to present a second data signal and a second indicator

signal in response to the first data signal, the first indicator signal and a second clock signal.